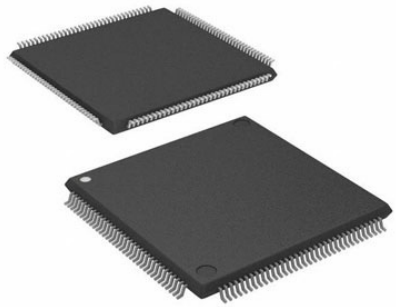
ADSP-21261SKSTZ150

Data Sheet

DSP, Floating Point, 32 / 40bit, 150 MHz, QFP, 144 Pins

Manufacturers	Analog Devices, Inc
Package/Case	LQFP-144
Product Type	Digital Signal Processors & Controllers - DSP, DSC
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for ADSP-21261SKSTZ150 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADSP-21261 is the lowest cost member of the third-generation of SHARC® programmable digital signal processors. A range of cost-sensitive applications such as voice recognition, medical appliances, measurement devices, high-quality audio, and automotive entertainment systems will benefit from the ADSP-21261's integration of large on-chip memory and diverse set of peripherals.

The ADSP-21261 is well suited for use in cost sensitive, signal processing applications.

The ADSP-21261 is based on the SHARC (SIMD) core that supports execution of 32-bit fixed-point and 32/40-bit floating-point arithmetic formats. With its core running at 150MHz (6.67 ns instruction cycle time), the ADSP-21261 is capable of executing complex Fast Fourier Transform (FFT) operations—1024-point complex FFT in 61us. The processor's single-instruction, multiple data (SIMD) mode effectively doubles the processor performance.

The ADSP-21261 offers a high level of integration, including 1 Mbit of on-chip dual-ported SRAM and 3Mbits of mask programmable ROM memory. This large on-chip dual-ported memory enables sustained processor and I/O performance without the need for external memory. System I/O is achieved through four full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 18 zero-overhead Direct Memory Access (DMA) channels delivering fast data transfers without processor intervention and an innovative Digital Audio Interface (DAI) which provides the user complete software control through its Signal Routing Unit (SRU).

Digital Audio Interface (DAI) for Simplified I/O System DevelopmentThe ADSP-21261 utilizes the Digital Audio Interface (DAI), an architecture that enables complete software programmability of various on-chip peripherals. The flexibility and ease-of-use of the SHARC programming model, combined with the DAI, allow manufacturers to deploy one hardware configuration into multiple product offerings with different I/O requirements.

Connections are made using the flexible Signal Routing Unit (SRU), a matrix routing group of pins that provides configurable and flexible connectivity between all DAI components and the SRU. The peripherals connected through the DAI are: a precision clock generator (PCG), an input data port (IDP), four SPORTS (serial ports), six flag inputs, six flag outputs, three timers and the SRU. The IDP provides an additional input path to the DSP core, configurable as 8 channels of receive serial data or as 7 channels of receive serial data and a single channel of up to a 20-bit wide parallel data. This level of integration enables the designer to take full advantage of a wide variety of peripherals without sacrificing the overall system performance.

CROSSCORE Development ToolsAll 3rd Generation SHARC Processors are supported by ADI's CROSSCORE brand of award winning development tools. The CROSSCORE components include the VisualDSP++™ software development environment, EZ-KIT Lite™ evaluation systems, and emulators.

VisualDSP++ is an integrated software development environment, allowing for fast and easy development, debug, and deployment. The EZ-KIT Lite evaluation system provides an easy way to investigate the power of the ADI family of processors and begin to develop applications. Emulators are available for PCI and USB host platforms for rapid on-chip debugging. Additional development tools and algorithms are available from an extensive third-party development community.

Note: The functional block diagram is available in the data sheet.

Features

150MHz (6.67 ns) SIMD SHARC Core, capable of 900MFLOPS peak performance

Code compatible with all SHARC Processors

Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point and 32-bit fixed-point data types

1Mbit on-chip dual-ported SRAM; 3Mbits mask-programmable ROM

4 independent Serial Ports - Supports: Standard DSP Serial mode, I2S mode, Left Justified Sample pair mode and TDM mode

18 Zero-overhead DMA channels

SPI compatible interface and a 16-bit Parallel Port

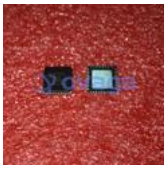
Digital Audio Interface (DAI)

Software configurable PLL providing many multiplier ratios

Four timers: 1 core and 3 general purpose timers

136-ball BGA (12mm x 12mm) and 144-lead LQFP (20mm x 20mm) packages available in Commercial and Industrial temp ranges

Related Products



ADUC7022BCPZ62

Analog Devices, Inc

LFCSP-40

ADUC7020BCPZ62

Analog Devices, Inc

LFCSP-40

ADUC841BSZ62-5

Analog Devices, Inc

QFP-52

ADUC841BSZ62-3

Analog Devices, Inc

QFP-52

ADUC831BSZ

Analog Devices, Inc

QFP-52

ADSP-BF527BBCZ-5A

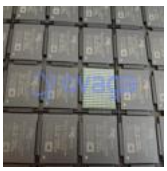
Analog Devices, Inc

BGA-208

ADSP-21369BBPZ-2A

Analog Devices, Inc

SBGA-256



ADSP-BF561SBBCZ-5A

Analog Devices, Inc

CSPBGA-256