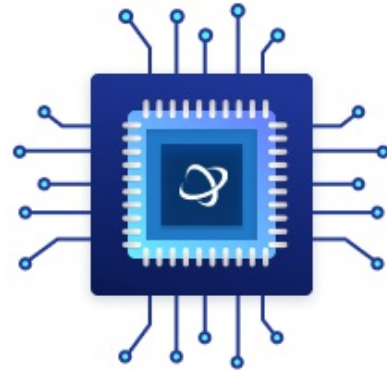


64 PORTS 12G SAS EXPANDER

Manufacturers	Microchip Technology, Inc
Package/Case	
Product Type	Interface ICs
RoHS	
Lifecycle	



Images are for reference only

Please submit RFQ for PM8056B-FEI or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

Features

SAS-3 T10 zoning for secure storage

Ultra low switching latency for improved system performance

SAS and SATA edge-buffering preserves customers' investment by improving performance with existing 3G and 6G drives

Table-to-table routing removes need for keyed connectors

Integrated Ethernet port for seamless interface to management entity

Integrated MIPS processor for enclosure management

Firmware compatible with Microchip SAS 3 Gbps and 6 Gbps SAS expanders and stand-alone enclosure management controllers

12G SAS signaling support for up to 10m mini-SAS HD passive copper cable

Optical SAS support

Early power off warning (EPOW) support

SAS and SATA edge-buffering support

Ultra-low switching latency to improve system performance

Quad SPI or parallel flash support; optional inline ECC on the parallel flash

T10 zoning support (up to 256 zones)

Port mirroring for system debug

Local bus data integrity protection

Real-time eye capture with enhanced BER eye mask and estimation

Non-disruptive zero down time firmware update support

Position-independent firmware image support to simplify firmware image management/download

Compatible enclosure management firmware architecture with SXP 3G/6G products

Real-time clock (1 μ S counter up to 35+ years)

Enhanced processing subsystem (MIPS 34Kc at 600 MHz)

Backward-compatibility with Microchip's 6G/3G SXP devices

High-Speed I/O

SAS-3 (12 Gbps, 6 Gbps, 3 Gbps, 1.5 Gbps) and SATA-3 (6 Gbps, 3 Gbps, 1.5 Gbps) operation

Support for up to 4K SAS addresses

Automated decision feedback equalizer (DFE) per SAS-3

Programmable continuous time linear equalizer for SATA-3

Supports spread-spectrum clocking (SSC) per SAS/SATA-3

Per-PHY configurable transmit and receive SSC

Per-PHY programmable transmit amplitude and emphasis

Integrated resistive termination

SAS 3.0-compliant back-channel training (SAS3 speed negotiation)

Peripheral Interfaces

4 UART interfaces for system monitoring and debugging

4 SGPIO interfaces (or additional TWI per SFF-8448)

Up to 81 GPIO pins

Eight dedicated two-wire interfaces (up to twelve total) for device configuration and control of external interfaces

16-bit local bus interface for connecting to NOR flash and SRAM

SPI, DSPI, and QSPI interface

10/100 Ethernet MAC port

JTAG and EJTAG interface

Statistics and Performance Monitoring

Per-port error counters for comprehensive diagnostic capability

Programmable PMON counters and interrupt generation

Per-link PRBS and CJPAT pattern generators and loop-backs for link integrity diagnostics

Real-time clock

Firmware Development Kit

Zoning configuration interface

SAM4/SPC4/SES3-compatible SES target with Enclosure Management Application reference design

SAS-3-compatible protocol stack in virtual SAS/SMP port

SSP/STP Initiator API supports communication with SSP/STP targets over SAS links

SMP routing management including topology discovery

Firmware download over multiple in-band and out-of-band interfaces

Expander diagnostics API

Disk spin-up control and disk qualification API

Peripheral drivers for TWI, UART, SGPIO, and Ethernet interfaces

TCP/IP enables management of the SXP 12G through remote network

Error detection, logging, and reporting

Wake up system through Ethernet or SAS port

Chiplink Diagnostic Utility

Supports advanced features for validation, characterization and debugging of Microchip expanders

Includes full SAS tool suite and a macro interface for user-authored animation scripts

Third Party Support

Green Hills MULTI development environment and EJTAG debugger

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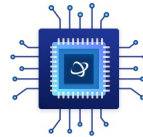
Green Hills MULTI development environment and EJTAG debugger

Related Products



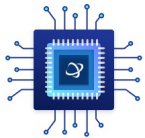
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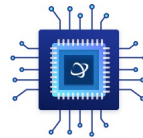
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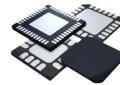
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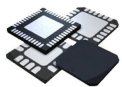
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