

16 BIT MCU/DSP 44LD 40MIPS 128KB FLASH, -40C to +85C, 44-TQFP, TRAY, Digitala signalprocessorer och kontroller (DSP, DSC) 16B DSC 128KB DMA 40MIPS

Manufacturers	Microchip Technology, Inc
Package/Case	TQFP-44
Product Type	Embedded Processors & Controllers
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for DSPIC33FJ128MC804-I/PT or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The dsPIC33F 16-bit device family employs a powerful 16-bit architecture, ideal for applications that rely on high-speed, repetitive computations, as well as control. The devices are pin compatible with the PIC24HJ family of devices, and share a very high degree of compatibility with the dsPIC30F family devices. This allows seamless migration options from/to PIC24F, dsPIC30F and dsPIC33F devices.

Features

Operating Range:

Up to 40 MIPS operation (@ 3.0-3.6V)

Industrial temperature range (-40°C to +85°C)

Extended temperature range (-40°C to +125°C)

High temperature range (-40°C to +150°C)

High-Performance DSC CPU:

Modified Harvard architecture

C compiler optimized instruction set

16-bit wide data path

24-bit wide instructions

Linear program memory addressing up to 4M instruction words

Linear data memory addressing up to 64 Kbytes

83 base instructions: mostly 1 word/1 cycle

Two 40-bit accumulators with rounding and saturation options

Flexible and powerful addressing modes: Indirect, Modulo and Bit-reversed software stack

16 x 16 fractional/integer multiply operations

32/16 and 16/16 divide operations

Single-cycle multiply and accumulate:

Accumulator write back for DSP operations

Dual data fetch

Up to ± 16 -bit shifts for up to 40-bit data

On-Chip Flash and SRAM:

Flash program memory (up to 32 Kbytes)

Data SRAM (2 Kbytes)

Boot and General Security for program Flash

Direct Memory Access (DMA):

8-channel hardware DMA

Up to 2 Kbytes dual ported DMA buffer area (DMA RAM) to store data transferred via DMA

Allows data transfer between RAM and a peripheral while CPU is executing code (no cycle stealing)

Most peripherals support DMA

Timers/Capture/Compare/PWM:

Timer/Counters, up to three 16-bit timers

Can pair up to make one 32-bit timer, 1 timer runs as Real-Time Clock with external 32.768 kHz oscillator, and Programmable prescaler

Input Capture (up to 4 channels): Capture on up, down or both edges, 16-bit capture input functions and 4-deep FIFO on each capture

Output Compare (up to 2 channels): Single or Dual 16-Bit Compare mode and 16-bit Glitchless PWM mode

Interrupt Controller:

5-cycle latency, 118 interrupt vectors, Up to 26 available interrupt sources

Up to 3 external interrupts, 7 programmable priority levels, and 5 processor exceptions

Digital I/O:

Peripheral pin Select functionality

Up to 35 programmable digital I/O pins

Wake-up/Interrupt-on-Change for up to 21 pins

Output pins can drive from 3.0V to 3.6V

Up to 5V output with open drain configuration

All digital input pins are 5V tolerant

4 mA sink on all I/O pins

System Management:

Flexible clock options: External, crystal, resonator, internal RC

Fully integrated Phase-Locked Loop (PLL) with Extremely low jitter

Power-up Timer

Oscillator Start-up Timer/Stabilizer

Watchdog Timer with its own RC oscillator

Fail-Safe Clock Monitor

Reset by multiple sources

Power Management:

On-chip 2.5V voltage regulator

Switch between clock sources in real time

Idle, Sleep and Doze modes with fast wake-up

Analog-to-Digital Converters (ADCs):

10-bit, 1.1 Msps or 12-bit, 500 Ksps conversion

2 and 4 simultaneous samples (10-bit ADC)

Up to 6 input channels with auto-scanning

Conversion start can be manual or synchronized with 1 of 4 trigger sources

Conversion possible in Sleep mode

Comparator Module:

Two analog comparators with programmable input/output configuration

CMOS Flash Technology:

Low-power, high-speed Flash technology

Fully static design

3.3V ($\pm 10\%$) operating voltage

Industrial and Extended temperature

Low power consumption

Motor Control Peripherals:

6-channel 16-bit Motor Control PWM

3 duty cycle generators

Independent or Complementary mode

Programmable dead time and output polarity

Edge-aligned or center-aligned

Manual output override control

1 Fault input

Trigger for ADC conversions

PWM frequency for 16-bit resolution (@ 40>

PWM frequency for 11-bit resolution (@ 40>

2-channel 16-bit Motor Control PWM:

1 duty cycle generator

Independent or Complementary mode

Programmable dead time and output polarity

Edge-aligned or center-aligned

Manual output override control

1 Fault input

Trigger for ADC conversions

PWM frequency for 16-bit resolution (@ 40>

PWM frequency for 11-bit resolution (@ 40>

Quadrature Encoder Interface module

Phase A, Phase B and index pulse input

16-bit up/down position counter

Communication Modules:

4-wire SPI (up to two modules):

Framing supports I/O interface to simple codecs

Supports 8-bit and 16-bit data

Supports all serial clock formats and sampling modes

I2C™with Full Multi-Master Slave mode support

7-bit and 10-bit addressing

Bus collision detection and arbitration

Integrated signal conditioning

Slave address masking

UART (up to two modules) with Interrupt on address bit detect and Interrupt on UART error

Wake-up on Start bit from Sleep mode

4-character TX and RX FIFO buffers

LIN bus support

IrDA® encoding and decoding in hardware

High-Speed Baud mode

Hardware Flow Control with CTS and RTS

Enhanced CAN (ECAN. module) 2.0B active

Up to eight transmit and up to 32 receive buffers

16 receive filters and three masks

Loopback, Listen Only and Listen All

Messages modes for diagnostics and bus monitoring

Wake-up on CAN message

Automatic processing of Remote Transmission Requests

FIFO mode using DMA and DeviceNet. addressing support

Parallel Master Slave Port (PMP/EPSP):

Supports 8-bit or 16-bit data

Supports 16 address line

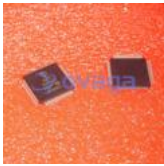
Programmable Cyclic Redundancy Check (CRC) Programmable bit

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