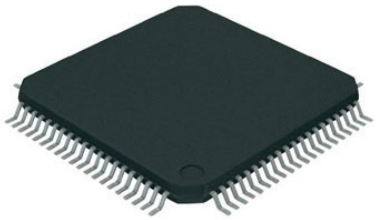
AD9461BSVZ

Data Sheet

Analogue to Digital Converter, 16 bit, 130 MSPS, Differential, Parallel, Single, 3.3 V

Manufacturers	Analog Devices, Inc
Package/Case	TQFP-100
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9461BSVZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADC requires 3.3 V and 5.0 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are CMOS or LVDS compatible (ANSI-644 compatible) and include the means to reduce the overall current needed for short trace distances.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data mode.

The AD9461 is available in a Pb-free, 100-lead, surface-mount, plastic package (100-lead TQFP/EP) specified over the industrial temperature range −40°C to +85°C.

Product Highlights

True 16-bit linearity.

High performance: outstanding SNR performance for baseband IFs in data acquisition, instrumentation, magnetic resonance imaging, and radar receivers.

Ease of use: on-chip reference and high input impedance track-and-hold with adjustable analog input range and an output clock simplifies data capture.

Packaged in a Pb-free, 100-lead TQFP/EP package.

Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of clock pulse widths.

OR (out-of-range) outputs indicate when the signal is beyond the selected input range.

Features

130 MSPS guaranteed sampling rate (AD9461-130)

78.4 dBFS SNR with 10 MHz input (3.4 V p-p input, 130 MSPS)

77.1 dBFS SNR / 85 dBc SFDR with 170 MHz

input (3.4V p-p input, 130 MSPS)

83 dBc SFDR with 225 MHz input(3.4V p-p input, 130 MSPS)

89 dBFS two-tone SFDR with 169 MHz and 170 MHz (130 MSPS)

60 fsec rms jitter

Excellent linearity = ±4.0 LSB typical

2.0 V p-p to 4.0 V p-p differential full-scale input

Buffered analog inputs

LVDS outputs (ANSI-644 compatible) or CMOS outputs

Data format select (offset binary or twos complement)

Output clock available

Application

MRI receivers

Multicarrier, multimode cellular receivers

Antenna array positioning

Power amplifier linearization

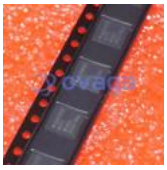
Broadband wireless

Radar

Infrared imaging

Communications instrumentation

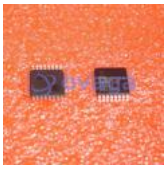
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64